We claim:

1. An ultracapacitor, comprising:

a semiconductor substrate;

N conductive layers on the substrate, where $N > 2$; and

N-1 dielectric layers formed between the conductive layers respectively.

2. The ultracapacitor of claim 1, wherein even numbered ones of the N conductive layers are connected to a first voltage and odd numbered ones of the N conductive layers are set to a second voltage.

3. The ultracapacitor of claim 2, wherein the N conductive layers store a distribution of charge corresponding to a difference between the first and second voltages.

4. The ultracapacitor of claim 1, wherein a uniform charge distribution is stored among the N conductive layers.

5. The ultracapacitor of claim 1, wherein a non-uniform charge distribution is stored among the N conductive layers.

6. The ultracapacitor of claim 1, wherein the N conductive layers have a same width.

7. The ultracapacitor of claim 1, wherein at least two of the N conductive layers have different widths.

8. The ultracapacitor of claim 7, wherein the N conductive layers include at least two adjacent conductive layers that have different widths.

9. The ultracapacitor of claim 1, wherein the N conductive layers include adjacent pairs of conductive layers and wherein the conductive layers in each pair have a same width.

10. The ultracapacitor of claim 9, wherein the widths of the conductive layers in each pair are different from the widths of the conductive layers in every other pair.

11. The ultracapacitor of claim 1, wherein the N conductive layers are equally spaced.

12. The ultracapacitor of claim 1, wherein the N conductive layers are spaced differently.

13. The ultracapacitor of claim 1, wherein the conductive and dielectric layers form a plurality of capacitors connected in parallel.

14. The ultracapacitor of claim 1, wherein the N-1 dielectric layers are at least partially made an oxide of hafnium, and oxide of zirconium, and a barium titanate powder.

15. The ultracapacitor of claim 14, wherein the oxide of hafnium has a dielectric constant k = 15, the oxide of zirconium has a k = 22, and the barium titanate powder has a k = 230.

16. An integrated circuit, comprising:

a first ultracapacitor; and

a second ultracapacitor connected in series to the first ultracapacitor.

17. The circuit of claim 16, further comprising:

a semiconductor substrate supporting both the first and second ultracapacitors.

18. The circuit of claim 16, wherein the first and second ultracapacitors each include:

a semiconductor substrate,

N conductive layers on the substrate, where N > 2, and

N-1dielectric layers formed between the conductive layers respectively.

19. The circuit of claim 18, wherein the N conductive layers form a plurality of capacitors connected in parallel.

20. The circuit of claim 16, wherein the first and second ultracapacitors are formed on stacked substrates.

21. A battery, comprising:

a semiconductor substrate;

N conductive layers on the substrate, where N > 2; and

N-1dielectric layers formed between the conductive layers respectively,

wherein the conductive and dielectric layers store a charge corresponding to a predetermined voltage.

22. The battery of claim 21, wherein the predetermined voltage falls within an operating voltage of an electronic device.

23. The battery of claim 22, wherein the electronic device is a portable computing device.

24. The battery of claim 22, wherein the electronic device is a communications device.

25. A semiconductor die, comprising:

N conductive layers on the substrate, where N > 2; and

N-1dielectric layers formed between the conductive layers respectively,

wherein the conductive and dielectric layers store a charge corresponding to a predetermined voltage.

26. The die of claim 25, wherein even numbered ones of the N conductive layers are connected to a first voltage and odd numbered ones of the N conductive layers are set to a second voltage.

27. The die of claim 26, wherein the N conductive layers store a distribution of charge corresponding to a difference between the first and second voltages.

28. The die of claim 25, wherein the conductive and dielectric layers form a plurality of capacitors connected in parallel.

29. The die of claim 25, wherein the parallel connection of capacitors powers a processor.

30. The die of claim 25, wherein the parallel connection of capacitors is included in one of a processor, a memory, a cache, a chipset, and an interface.